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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/810,038 | 03/26/2004 | Rajesh Manapat | CD03191 | 8446 |

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| EXAMINER | |
|---|---|
| LE, THONG QUOC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/810,038 | MANAPAT ET AL. | |
| | Examiner | Art Unit | |
| | Thong Q. Le | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-13 and 15-20* is/are rejected.

7)☒ Claim(s) *7 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-20 are presented for examination.

### *Information Disclosure Statement*

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 3/26/2004.

3. Information disclosed and list on PTO 1449 was considered.

### *Specification*

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Objections*

5. Regarding claim 10, claim discloses the number N is no less than 2. Since claim 9, the number N is defined greater than 1, and none of number between 1 and 2. Therefore, claim 9 should be amended for more clearly or have to be canceled.

### *Claim Rejections - 35 USC § 102*

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-6,8-13, 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yagishita et al. (U.S. Patent No. 6,728,157).

Regarding claims 1,9, Yagishita et al. disclose a memory device (Figure 1), comprising:

at least a first memory cell array (BLK0, ABSTRACT) coupled to a read data bus (RDB) that outputs read data and coupled to a separate write data bus (WDB) that inputs write data, the at least first memory cell array accessing read data in response to a first type edge of a first clock and latching write data on at least the first type edge of the first clock (Column 4, lines 40-67, Column 5, lines 1-9, Figures 3-4, RDP) ; and

at least a second memory cell array (BLK1, ABSTRACT) coupled to the read data bus (RDB) and coupled to the write data bus (WDB), the at least second memory cell array accessing read data in response to a first type edge of a second clock and latching write data on at least the first type edge of the second clock, the second clock

being phase shifted with respect to the first clock by less than $180^0$ (Column 4, lines 40-67, Column 5, lines 1-9, Figures 3-4, RDP).

Regarding claims 2-6, 9-13, Yagishita et al. disclose wherein the first and second memory cell arrays comprise sections of n x m memory cells, and the write data bus includes m input data lines (Figure 1, DQA, DQB0, and wherein the first and second memory cell arrays comprise static random access memory (SRAM) cells (Column 4, lines 43), and wherein the second clock is synchronous with, and phase shifted by about $90^0$ with respect to the first clock (Figures 4-5), and the first memory cell array latches write data on both the first and second type edges of the first clock; and the second memory cell array latches write data on both the first and second type edges of the second clock (Column 4, lines 40-54), and an address bus different than the read data bus and write data bus (Figure 1, ADR19-1); a first address latch (Figure 1, 14) coupled between the address bus and the first memory cell array that latches an address value on the address bus in response to the first type edge of the first clock, and outputs an internal address, and a second address latch coupled between the first address latch and the second memory cell array that latches the internal address value in response to the first type edge of second clock (Figure 1, 300, Column 4, lines 60-67, Column 5, lines 1-67), and an address bus (Figure 1, ADR) different than the read data bus and write data bus; a first write address decoder (Figure 1, 12) coupled to the first memory cell array, a first write address register (Figure 2, 44) coupled to the address bus having an output coupled to a first write address decoder, a second write address decoder (Figure 2, 44) coupled to the second memory cell array and a second write

address register coupled to the first write address register having an output coupled to a second write address decoder (Figure 3).

Regarding claims 15-20, the apparatus discussed above would perform the method claims 15-20.

***Allowable Subject Matter***

8. Claims 7, 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 7, 14 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Yagishita et al. (U.S. Patent No. 6,728,157), and others, does not teach the claimed invention having a multiplexer having one input coupled to the first memory cell array and another input couple to the second memory cell array that coupled read data at least four times the rate of the first clock signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER